Low Cost AC-DC 5.0 W Adapter with NCP1215

Prepared by: Petr Lidak
ON Semiconductor

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APPLICATION NOTE

INTRODUCTION

The goal of this paper is to present a design example of a 5.0 W rated AC−DC adapter for consumer products like the mobile phone, walkman, walkie−talkie, MPEG players, digital camera, various battery chargers, etc. This sort of adapter is specified at very low cost to not hamper the selling price of the above products. However, this does not imply that an adapter designer has to sacrifice safety, precision and standby performance.

By implementing the NCP1215 dedicated for switched−mode power supply (SMPS) control one can build an adapter that can meet all those requirements. This can be achieved with the help of the following NCP1215 basic features:

- **Current Mode Control:** Cycle−by−cycle primary current observation is helping to prevent any significant primary overcurrent which would cause transformer's core saturation and consequent serious power supply failure.
- **Negative Primary Current Sensing:** Negative current sensing offers an elegant way to drive a MOSFET without a) reducing the available gate−source voltage as the sense resistor voltage grows−up b) deteriorating the voltage image of the primary current via the strong turn−on pulse due to the input capacitance. The programming resistor offers another degree of freedom when selecting the voltage across the sense resistor. Furthermore, the programming resistor together with pin capacitance forms low−pass filter which cleans up the residual noise generated at main switch turn−on by charging process of all parasitic capacitances included in transformer's windings, snubbers, output diode, and printed circuit board traces.
- **Very Low Start−up Current:** The patented internal supply block is specially designed to offer a very low current consumption during start−up. It allows the use of a very high value external start−up resistor, greatly reducing dissipation, efficiency and standby power consumption.
- **Frequency Foldback:** Since the switch−off time increases when power demand decreases, the switching frequency naturally diminishes in light load conditions. This helps to minimize switching losses and offers excellent standby power performance.
- **Secondary or Primary Regulation:** The feedback loop arrangement allows secondary or primary side regulation without significant additional external components.

By exploitation of all above−mentioned features one can build an AC−DC adapter with the NCP1215 in quite an efficient way.

Since the operation of the NCP1215 differs significantly from the standard fixed frequency current mode controllers, a more detailed explanation of the operation will follow.

Summary of NCP1215 Operation

There can be identified two basic categories of the power losses within any SMPS. These are the conduction and switching losses. The conduction losses become dominant at rather high output power levels. But the situation can completely change when the demanded output power decreases to low or standby level. In this situation, switching losses become a major contributor of the power leak.

This situation is typical for standard control IC's working with fixed switching frequency. It can be even worse for SMPS based on very popular self−oscillating concept where at light load condition the switching frequency usually escalates to very high values.

The idea behind the NCP1215 operation is to reduce the switching losses of the SMPS during this light load or standby operation. This can be simply ensured by keeping constant primary ON time. As a result, output regulation is obtained by adjusting the OFF time duration. This is exactly the way the NCP1215 is working. Experimental results have proven the concept with an excellent standby consumption in no−load conditions.

If the switching frequency decreases as the output power demand goes down, it will move in the opposite direction when responding to an output increase. In light load conditions, the frequency can go really low and operation within the audible range is feasible. Since the peak primary current is set to maximum for the working range, power pulses at audio frequency induce an audible whistle coming mainly from the transformer. The power supply user does not appreciate this whistle.

The solution is a compromise between those two extremes. The result is the control apparatus that has in light load condition fixed peak primary current to a certain portion of the maximum value. This little current reduction helps to get away from audio range and to lower the level of the audio noise. It increases the standby self−consumption, but not significantly. For higher output power levels the peak primary current continuously increases up to its maximum.

The resulting block diagram of the internal structure can be seen in Figure 1. From that figure the basic element of the idea described above is the current source connected to the CS pin. Its value varies between 12.5 and 50 μA depending on the signal coming from the feedback block. The resulting transfer characteristic can be seen in Figure 2.

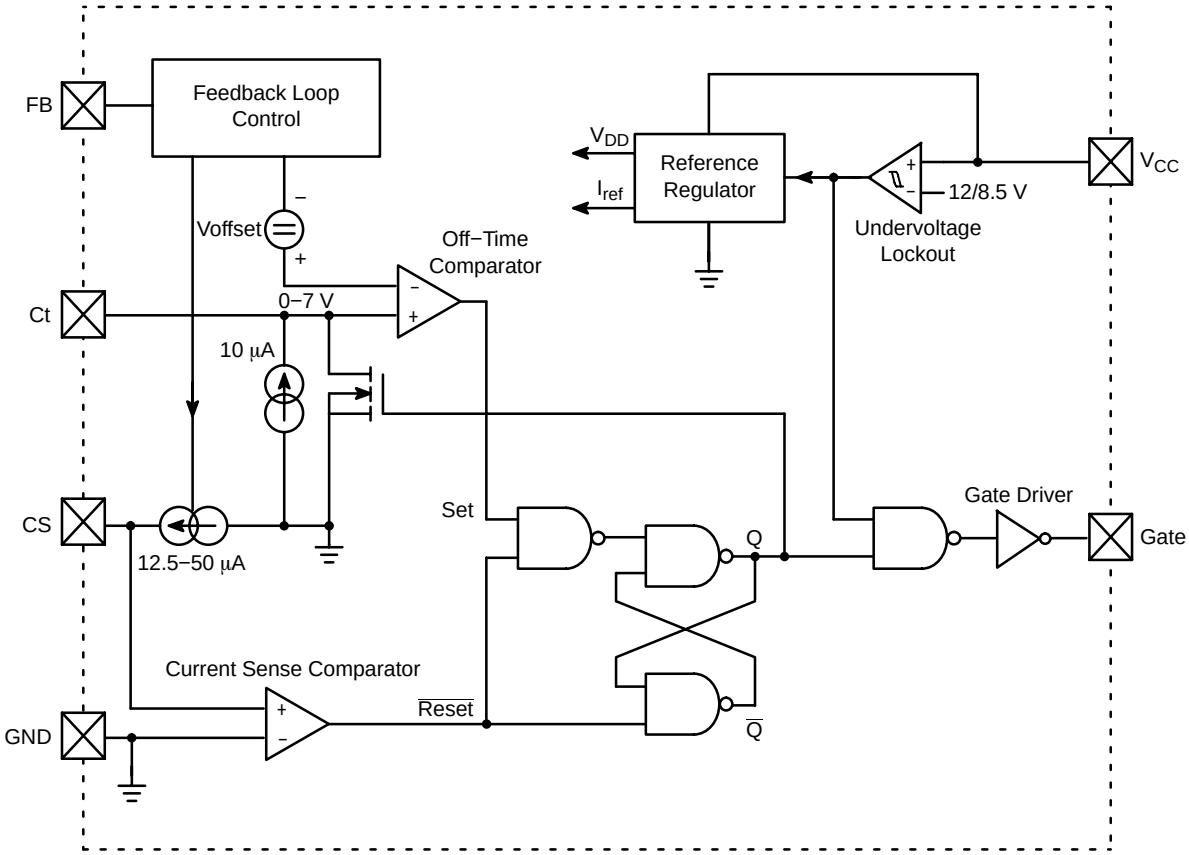

Figure 1. Representative Block Diagram

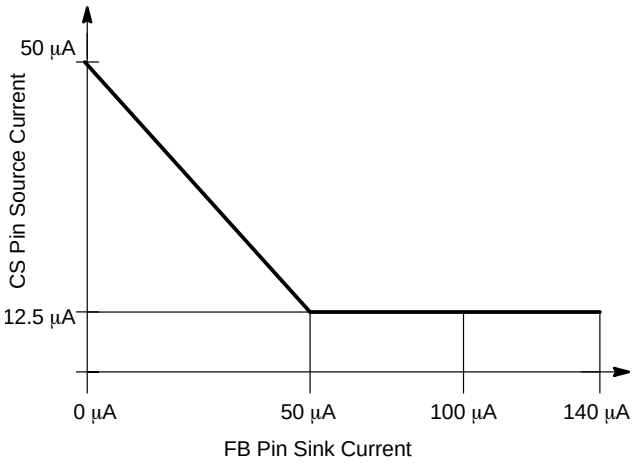

Figure 2. Current Sense Regulation Characteristic

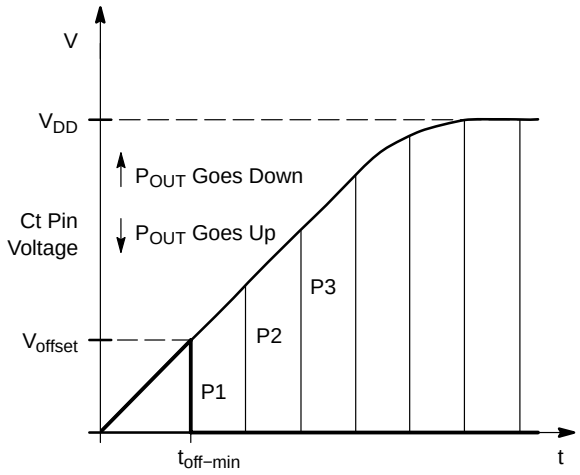

Figure 3. C_t Pin Voltage ($P_{out}1 > P_{out}2 > P_{out}3$)

The variable current source dictates through the CS pin and external resistors the peak primary current.

The OFF time is generated by a timer consisting of the OFF time comparator, a 10 μA current source, a discharge switch and the external timing capacitor. The signal that can be observed on the CT pin has the shape as depicted in Figure 3.

Due to this shape the IC can allow an OFF time of several seconds or can even stop the switching.

This was the basic summary of the IC operation. The practical design of the AC−DC adapter will follow.

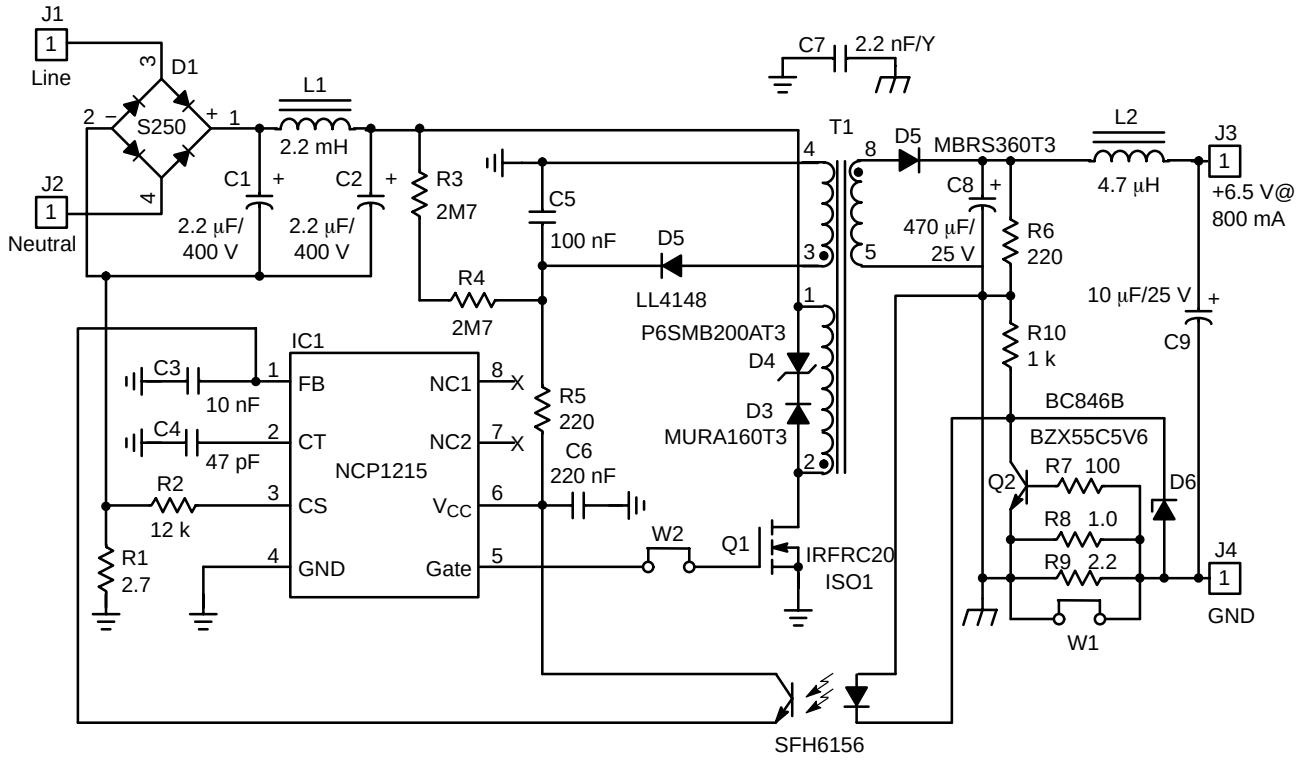

Figure 4. Schematic Diagram of the AC/DC 5.0 W Adapter with NCP1215

The 5.0 W AC−DC Adapter Board

The adapter depicted in Figure 4 has the maximum and performance ratings:

Output Voltage	6.5 VDC
Output Current	0.8 A
Min. Input Voltage	90 VAC
Max. Input Voltage	275 VAC
Max. Switching Frequency	75 kHz

Using the AC specification of the input voltage the bulk capacitor voltage range can be calculated as follows:

$$V_{bulk-min} = V_{AC-min}\sqrt{2} = 90 \cdot \sqrt{2} = 127\ VDC$$

$$V_{bulk-max} = V_{AC-max}\sqrt{2} = 265 \cdot \sqrt{2} = 375\ VDC$$

The power conversion efficiency of 80% for this size adapter would be appropriate. The input power then can be estimated as follows:

$$P_{in} = \frac{V_{out} \cdot I_{out}}{\eta} = \frac{6.5 \cdot 0.8}{0.8} = 6.5\ W$$

The average value of the input current at minimum input voltage is:

$$I_{in-avg} = \frac{P_{in}}{V_{bulk-min}} = \frac{6.5}{127} = 51.2\ mA$$

The suitable reflected primary winding voltage for 600 V rated MOSFET switch is:

$$V_{flbk} = 600\ V - V_{bulk-max} - V_{spike}$$
$$= 600 - 375 - 100 = 125\ V$$

Using calculated flyback voltage the maximum duty cycle can be calculated:

$$\delta_{max} = \frac{V_{flbk}}{V_{flbk} + V_{bulk-min}} = \frac{125}{125 + 127} = 0.496 = 0.5$$

The following equation determines peak primary current:

$$I_{ppk} = \frac{2 \cdot I_{in-avg}}{\delta_{max}} = \frac{2 \cdot 51.2 \cdot 10^{-3}}{0.5} = 204.7\ mA$$

Transformer Design

Using a specified maximum switching frequency of 75 kHz at nominal output power the primary inductance can be calculated:

$$L_p = \frac{V_{bulk-min} \cdot \delta_{max}}{I_{ppk} \cdot f_{sw-max}} = \frac{127 \cdot 0.5}{0.2047 \cdot 75 \cdot 10^3} = 4.14\ mH$$

The highest switching frequency occurs at the highest input voltage and its value can be estimated as follows:

$$f_{max-high} = f_{max-low}\frac{V_{bulk-max}}{V_{bulk-min}}\delta_{max}$$
$$= 75 \cdot 10^3\,\frac{375}{127}\,0.5 = 110.7\ kHz$$

The EF16 core for transformer was selected. It features a cross−section area A_e = 20.1 mm^2. The N67 magnetic allows to use maximum operating flux density B_{max} = 0.28 Tesla.

The number of turns of the primary winding is:

$$n_p = \frac{L_p \cdot I_{ppk}}{B_{max} \cdot A_e} = \frac{4.14 \cdot 10^{-3} \cdot 0.2047}{0.28 \cdot 20.1 \cdot 10^{-6}} = 150\ turns$$

The A_L factor of the transformer's core can be calculated:

$$A_L = \frac{L_p}{(n_p)^2} = \frac{4.14 \cdot 10^{-3}}{(150)^2} = 184\ nH$$

For an adapter output voltage of 6.5 V, the number of turns for the secondary winding can be calculated accounting Schottky diode for output rectifier as follows:

$$n_s = \frac{(V_s + V_{fwd})(1 - \delta_{max})n_p}{\delta_{max} \cdot V_{bulk-min}}$$
$$\frac{(6.5 + 0.5)(1 - 0.5)150}{0.5 \cdot 127} = 8.26 = 8\ turns$$

Using the calculated number of the secondary winding turns the number of turns for auxiliary winding can be calculated:

$$n_{aux} = \frac{(V_{aux} + V_{fwd})}{V_s + V_{fwd}} \cdot n_s$$
$$= \frac{(14.5 + 1)}{6.5 + 0.5} \cdot 8 = 17.7 = 18\ turns$$

Primary Current Control

The peak primary current is known from initial calculations. The current sense method allows choosing the voltage drop across the current sense resistor. Let's use a value of 0.5 V. The value of the current sense resistor can then be evaluated as follows:

$$R_{CS} = \frac{V_{CS}}{I_{ppk}} = \frac{0.5}{0.2047} = 2.442\ \Omega = 2.7\ \Omega$$

The voltage drop across the sense resistor needs to be recalculated:

$$V_{CS} = R_{CS} \cdot I_{ppk} = 2.7 \cdot 0.2047 = 0.553\ V$$

Using the above results the value of the shift resistor is:

$$R_{shift} = \frac{V_{CS}}{I_{CS}} = \frac{0.553}{50 \cdot 10^{-6}} = 11.06\ k\Omega = 12\ k\Omega$$

OFF Time Control

The value of the timing capacitor for the off time control has to be calculated for minimum bulk capacitor voltage since at this condition the converter should be able to deliver the specified maximum output power. The value of the timing capacitor is then given by the following equation:

$$C_T = \frac{\frac{1}{f_{sw}} - \frac{L_p \cdot I_{ppk}}{V_{bulk-min}}}{1.2 \cdot 10^6}$$

$$= \frac{\frac{1}{75 \cdot 10^3} - \frac{4.14 \cdot 10^{-3} \cdot 0.2047}{127}}{0.12 \cdot 10^6} = 55.5\ pF$$

Taking into account the parasitic internal capacitance connected to the CT pin the external timing capacitor should be around 10 pF smaller. The value of 47 pF for the external timing capacitor would be appropriate.

Start−up Circuit

The value of the start−up resistor for corresponding to a start−up time of 300 ms and a Vcc capacitor of 300 nF is following:

$$R_{start-up} = \frac{V_{bulk-min}}{C_{Vcc}\frac{V_{start-up}}{t_{start-up}} + I_{CC-start}^{MAX}}$$

$$= \frac{127}{200 \cdot 10^{-9}\frac{12}{0.2} + 10 \cdot 10^{-6}}$$

$$= 5.77\ M\Omega = 5.6\ M\Omega$$

Feedback Loop

The output voltage is sensed on the secondary side by series connection of the Zener diode and the LED diode inside the optocoupler. Resistor R6 reduces the maximum current that can possibly flow through the optocoupler's diode. Resistor R10 introduces a bias current for Zener diode to move its operating point toward steeper part of the V−A characteristic.

A simple circuit consisting of the sensing resistor R8//R9, resistor R7 and transistor Q2 also implements an output current limitation. The current limitation can be disabled by jumper W1.

The control signal from secondary side is being delivered to the primary side through the optocoupler ISO1. The optocoupler injects a current from supply capacitor to feedback pin 1. Capacitor C3 is a bypass capacitor against the high frequency noise pick−up.

Bill of Materials

C1	2.2 μF/400 V
C2	2.2 μF/400 V
C3	10 nF, C0805
C4	47 pF, C0805
C5	100 nF, C0805
C6	220 nF, C0805
C7	2.2 nF/Y1
C8	470 μF/25 V
C9	10 μF/25 V
D1	S250
D2	LL4148
D3	MURA160T3, ON Semiconductor
D4	P6SMB200AT3, ON Semiconductor
D5	MBRS360T3, ON Semiconductor
D6	BZX55C5V6
IC1	NCP1215, ON Semiconductor
ISO1	SFH6156
L1	2.2 mH
L2	4.7 μH
Q1	IRFRC20
Q2	BC846B
R1	2.7, R0805
R2	12 k, R0805
R3, R4	2M7, R1206
R5	220, R0805
R6	220, R1206
R7	100, R1206
R8	1, R1206
R9	2.2, R1206
R10	1.0 k, R1206
T1	A9765−A, Coilcraft, 1102 Silver Lake Road CARY IL 60013 Email: info@coilcraft.com Tel.: 847−639−6400 Fax: 847−639−1469

PCB Layout

The NCP1215 is designed to have low power consumption when operating. For this reason the output currents injected out of the CS and CT pin is pretty low. Also the FB pin can be affected. Therefore proper printed circuit board layout is essential for a reliable operation of the converter in the whole operating range.

It is important to ensure good grounding technique and keep all high frequency current loop and high voltage areas as small as possible to avoid both magnetic and electric field radiations. The PCB layout can be seen in Figure 5.

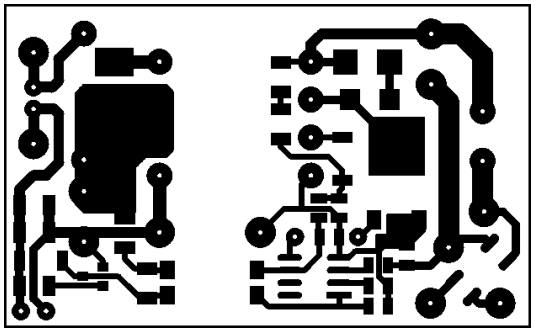

Figure 5. Printed Circuit Board Layout − Bottom Side

The top side is assembled with through hole components only. To locate those components the picture of the related silkscreen can be seen in Figure 6.

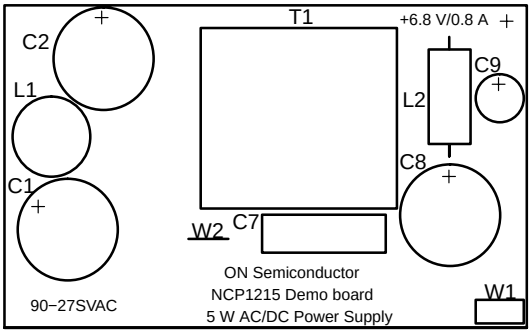

Figure 6. Silkscreen − Top Side

The bottom side is dedicated for SMD components. Figure 7 shows their positions.

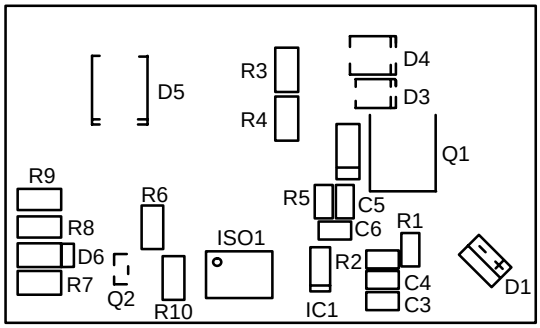

Figure 7. Silkscreen − Bottom Side

The physical dimensions of the board are 52.5*32.5 mm.

Practical Results

The application was measured at different conditions. The following pictures depict the typical waveforms at several most important points.

Figure 8 demonstrates the control signals at current sense pin CS (middle trace) and OFF−time timing capacitor's voltage (bottom trace) connected to pin CT. The gate driver output is depicted on the top trace for proper synchronization. The picture was captured at minimum input voltage of 127 VDC and nominal load.

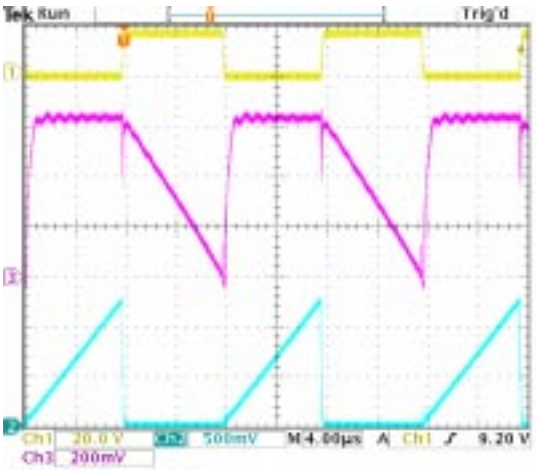

Figure 8. CS and CT Pin Voltage at 127 VDC and Full Load

Figure 9 shows the same waveforms but at no load condition.

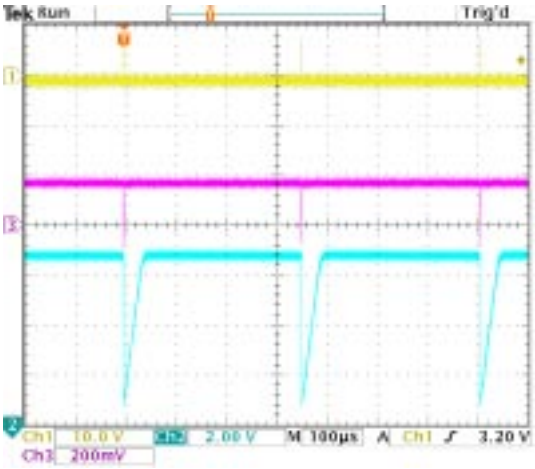

Figure 9. CS and CT Pin Voltage at 127 VDC and No Load

Figure 10 demonstrates the start−up sequence of the supply voltage at 127 VDC input voltage.

The top trace is the gate driver voltage. The bottom trace is the IC supply voltage measured on the VCC pin.

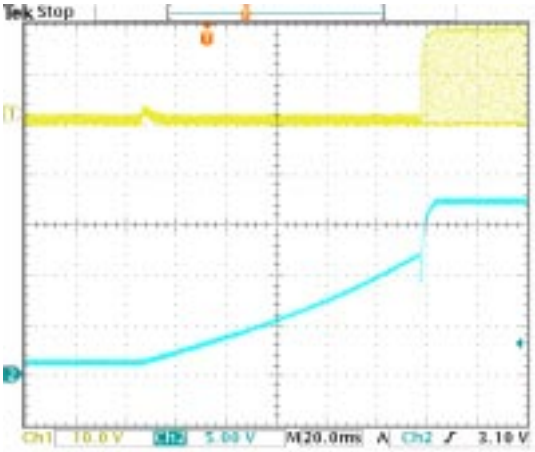

Figure 10. Supply Voltage Start−Up at 127 VDC

The same situation but at input voltage of 375 VDC is depicted in Figure 11.

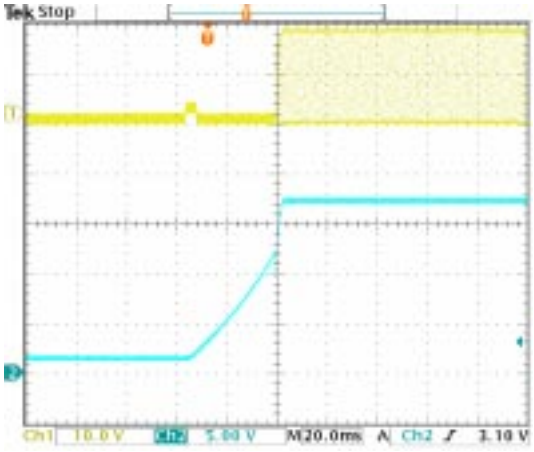

Figure 11. Supply Voltage Start−Up at 375 VDC

Since the adapter has incorporated the output current limitation, Figure 12 shows the output V−A characteristics.

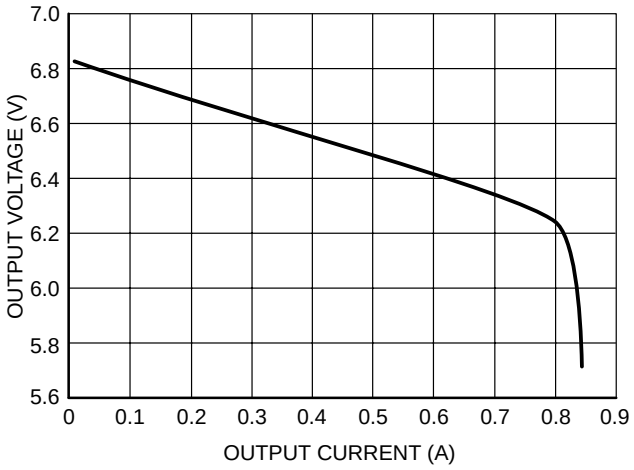

Figure 12. Output V−A Characteristics

The switching frequency variation over the operating load range is essential for NCP1215 operation. Figure 13 demonstrates the operation of the variable OFF−time block and also frequency compression at 127 VDC.

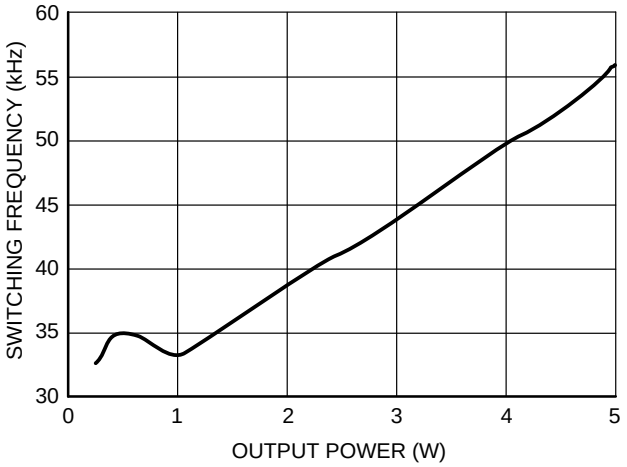

Figure 13. Switching Frequency vs. Output Power at 127 VDC

The dependency of the switching frequency on the input voltage can be estimated when comparing Figure 13 with Figure 14.

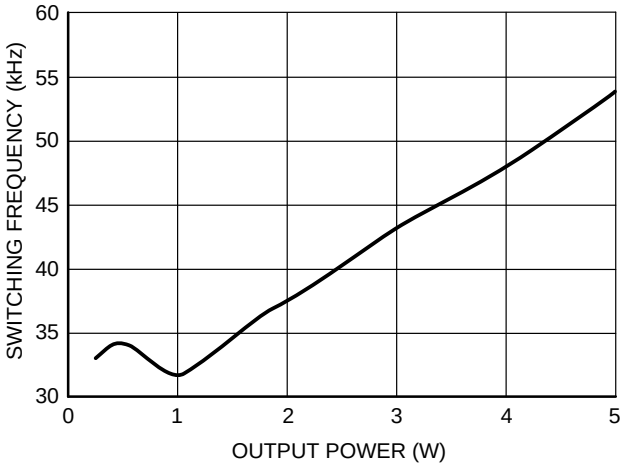

Figure 14. Switching Frequency vs. Output Power at 375 VDC

One of the most important parameters that characterize the power supply is the power conversion efficiency. Figure 15 shows achieved results at low line and Figure 16 at high line.

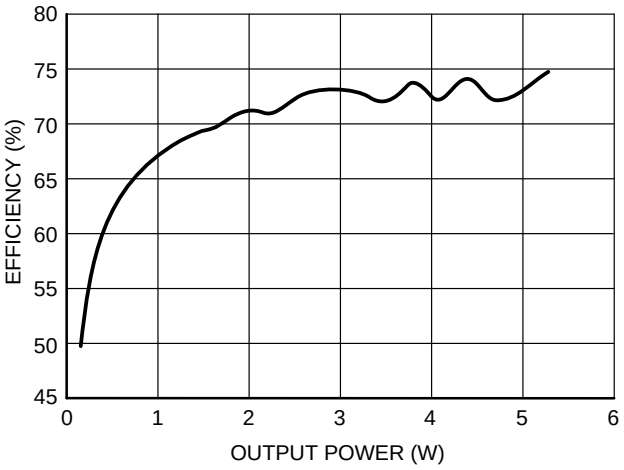

Figure 15. Power Conversion Efficiency at 127 VDC

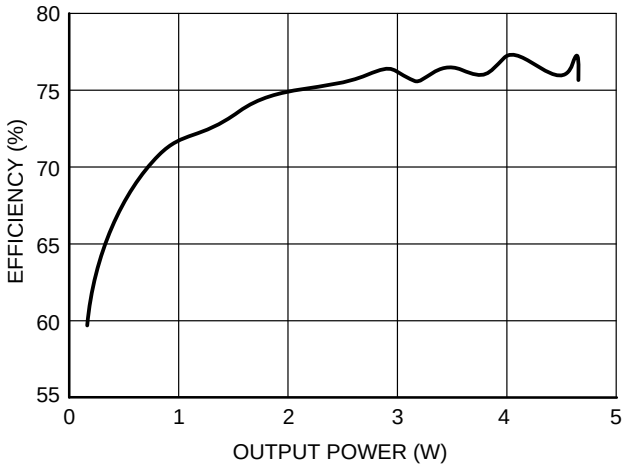

Figure 16. Power Conversion Efficiency at 375 VDC

Last but not least the parameter one can be interested in is the power consumption at no−load condition. Due to the frequency fold−back the achieved values are outstanding. At low line the power supply consumed only 20.3 mW and at high line due to the increased power loss in start−up resistors the consumption increased up to 57.7 mW.

Gate−Source Resistor Design Guidelines

In some applications, there is a need to wire a resistor between the MOSFET gate and source connections. This can preclude an eventual MOSFET destruction if, in the production stage, the converter is powered whilst the gate is left unconnected. However, dealing with an extremely low startup current implies a careful selection of the gate−source resistance. With the NCP1215, the gate−source resistor must be calculated to allow the growth of the V_{CC} capacitor to 4.0 V in order to not interfere with the power−on sequence. The following equation helps deriving Rgate−source, accounting for the minimum rectified input voltage and the startup resistor: Vin_{min} x Rgate−source/(Rgate−source + Rstartup) $>$ 4.0 V. If we take a Vin_{min} of 100 VDC, a startup resistor of 4.0 MΩ, then Rgate−source equals 180 kΩ as a minimum normalized value.

Notes

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